Shenzhen Hi-Link Electronic Co., Ltd.

Radar module HLK-LD6002C User Manual

CONTENTS

1. Device overview

1.1. Features

- Integrated PLL, Transmitter, Receiver, Baseband and ADCs
- Operating Frequency: 57 to 64GHz
- 2-Transmit, 2-Receive Channels
- Ultra-Accurate Chirp (Timing) Engine Based on Fractional-N PLL
- Tx Power @ Single Channel: 12dBm
- 57 to 65GHz Phase Noise@1MHz offset: -91dBc/Hz
- Rx Noise Figure: 11dB
- RF Built-in self-test (BIST) module, Self-calibrated System Across Frequency and Temperature
- ARM® Cortex®-M3 Core
- Built-in Digital Signal Process, including FIR, FFT and etc.
- Built-in FMCW Chirp generation
- Available IOs:
  --- 1 SPI Channels
  --- 1 CAN2.0/CAN-FD
  --- 3 UARTs
  --- 1 I2Cs
  --- Interface for analog IF output
- Power management with low power mode.
- Digital I/O voltage 3.3V
- Clock Source
  --- 50.0MHz Oscillator or Crystal
  --- Support external 32.768KHz crystal.
  --- Internal RC Oscillator, 32KHz +/- 20%
- Easy hardware design with 0.5mm pitch, 113-pin and 6.75mm x 6.75mm x 0.49mm fanout BGA package for small formfactor size

1.2. Applications

- Respiratory rate monitoring
- Human persistence monitoring
- Gesture recognition
- Low power carpark monitoring

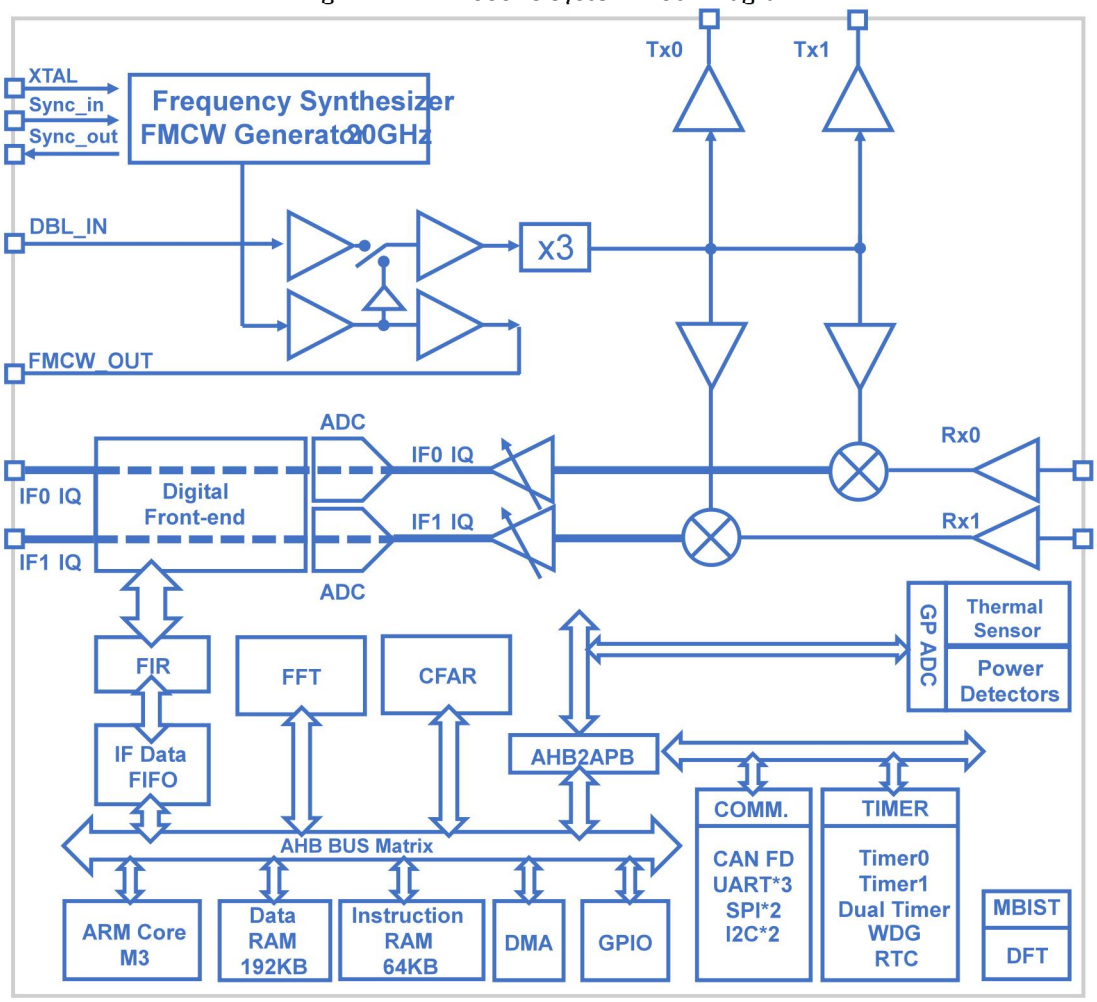
1.3. Description

HLK-LD6002C device has integrated 2 transmit and 2 receive channels, IQ down-conversion mixers, a RF VCO, a Fractional-N PLL, frequency tripler, built-in digital signal processing units, including FIR, FFT and other radar signal processing function blocks. The device includes an ARM® Cortex®-M3 Core based processor subsystem, which is responsible for radio chip configuration, control, calibration and data communications. The device is provided with a complete platform including reference design, software drivers, API guides and user documentations. The device also supports cascade-mode operation for applications that need higher accuracy and long range.

1.4. System Block Diagram

The detail system block diagram is shown in Fig. 1.1

Fig. 1.1 HLK-LD6002C System Block Diagram



2. Specifications

2.1. Absolute maximum ratings (1)

Table 2.1 Absolute Maximum Ratings

Signal Name	Signal description	Max Ratings		Unit
		Min	Max	
VDD_RF	RF power	0	1.45	V
VDD	Digital 1.2V supply	0	1.4	V
VDD12	Internal 1.2V LDO output	0	1.4	V
AVDD18_PLL	Internal PLL Power supply	0	2.75	V
AVDD18_PLL_VCO	Internal VCO Power	0	2.75	V
AVDD18_BB1	Internal Baseband1 Power	0	2	V
AVDD18_BB2	Internal Baseband2 Power	0	2	V

VDD33	Analog 3.3V Power	0	3.63	V
DVDD33	Digital 3.3V Power	0	3.63	V
CLKP, CLKN	Input ports for reference crystal	-0.5	2	V
Clamp current	Limit clamp current through the internal diode protection of the I/O	-20	20	mA
T_J	Operating junction temperature range	-40	125	°c
T_{STG}	Storage temperature range after soldered onto PC board	-55	150	°c

(1) Stress beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods of time may affect device reliability and lifetime

2.2. ESD ratings

Table 2.2 ESD Ratings

Signal description		Value	Unit
V(ESD)	Human-body model, HBM	±2000	V
	Charged-device model, CDM	±500	

2.3. Recommended operating conditions

Table 2.3 Recommended Operating Conditions

Signal Name	Signal description	Max Ratings			Unit
		Min	Nom	Max	
VDD_RF	RF power supply	1.15	1.35	1.45	V
VDD	Digital 1.2V Power	1.08	1.2	1.32	V
VDD12	Internal output 1.2V Power	1.08	1.2	1.32	V
AVDD18_PLL	Internal PLL Power Supply	2	2.5	2.75	V
AVDD18_PLL_VCO	Internal VCO Power Supply	1.7	1.8	1.9	V
AVDD18_BB1	Internal Baseband1 Power	1.7	1.8	1.9	V
AVDD18_BB2	Internal Baseband2 Power	1.7	1.8	1.9	V
DVDD33	3.3V, for GPIO interface	3	3.3	3.6	V
AVDD33	3.3V, for analog PLL, ADC	3	3.3	3.6	V
Analog module VIH	Voltage Input High (1.2V mode)	1.1			V
	Voltage Input High (3.3V mode)	2.5			
Analog module VIL	Voltage Input Low (1.2V mode)	0.3			V
	Voltage Input Low (3.3V mode)	0.8			
CLKP, CLKN	Voltage Input High	1.2			V
	Voltage Input Low	0.2			
MCU	Voltage Input High (3.3V mode)	2.5			V

	Voltage Input Low (3.3V mode)	0.6	V

2.4. Power supply specifications

Table 2.4 Power Supply SPEC

Voltage Define	1.35V	1.8V	3.3V
Supply SPEC	RF	Analog	GPIO, analog and digital part

2.5. Power consumption summary (2)

Table 2.5 Power Consumption Summary

Signal Name	Signal description	Max Ratings			Unit
		Min	Nom	Max	
VDD_RF	1.35V, power for 60GHz RF			600	mA
VDD	1.2V, for Digital Core		15		
DVDD33	3.3V, for GPIO interface		40		
AVDD33	3.3V, for analog circuits		210	250	

(2) The data is based on IC test data (10 pcs) under maximum output power on TX mode and RX mode at the same time

2.6. RF & IF specification

Table 2.6 RF Specifications

Parameter		Min	Nom	Max	Unit
SYS	Rx Baseband Frequency	0.1		4	MHz
	RF Frequency range	57	60	65	GHz
RF TX	Output Power		12		dBm
	In-band spur suppression		-50		dBc
	RF Phase Noise@1MHz		-91		dBc/Hz
RF RX	Reflection coefficient		-10		dB
	Receive Noise Figure		11		dB
	In- band spur suppression		-50		dBc
RX IF	TIA dynamic range (6dB/step)	0		18	dB
	High Pass Filter Conner Frequency	100		300	KHz
	Low Pass Filter Conner Frequency	2	4	10	MHz
	ADC sampling rate (real)			7.14	MSps
	ADC sampling rate (complex)			7.14	MSps
	ADC resolution		12		Bits
	Single end IF signal to ADC	0		800	mVpp
	VGA dynamic range (2dB/step)	0		40	dB
Local Oscillator	Frequency range	19		21.7	GHz
	Ramp rate		50		MHz/μs
	Input Local Oscillator Power	-15	-10	0	dBm

	Output Local Oscillator Power	0	2	4	dBm

2.7. MCU specification

Table 2.7 CPU Specifications

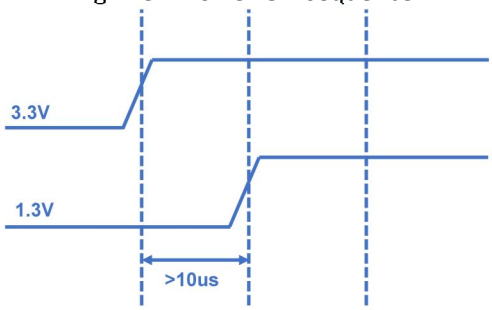
Parameter		Min	Mid	Max	Unit
ARM® Cortex®-M3 Core	Clock Speed		50	100	MHz
	ROM			32	KB
	Instruction RAM			64	KB
	Data RAM			192	KB

2.8. Timing and switching characteristics

2.8.1 Power supply sequencing

The HLK-LD6002C device expects the power on sequence as shown in Fig. 2.8.1.

Fig. 2.8.1 Power ON sequence



2.8.2 Input clock source specifications

A 50MHz crystal or external oscillator is used as the clock source.

Fig. 2.8.2 shows the crystal implementation. Table 2.8.2.1 lists the electrical characteristics of the required crystal.

Table 2.8.2.1 Crystal Electrical Characteristics

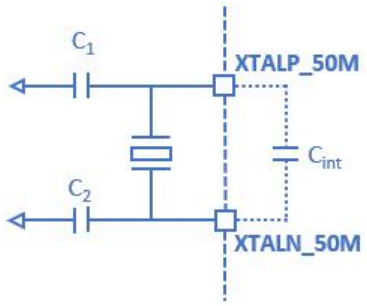
Name	Description	Min	Mid	Max	Unit
Reference Frequency	Crystal frequency		50		MHz
Temperature range	Operation temperature range	-40		125	℃
Frequency tolerance	Note (1)	-200		200	ppm
Load capacitance	Crystal load capacitance		8	12	pF
ESR	Effective Resistance			50	Ω

(1) Includes frequency tolerance, frequency stability over operating temperature range, aging and frequency pulling due to incorrect load capacitance of the crystal.

The load capacitors, C_1 and C_2 should be determined based on Equation 2.8.2, where C_L is the load capacitance in crystal specification provided by the manufacturer. C_{1p} and C_{2p} are the parasitic capacitances on the PCB traces. The crystal and load capacitors should be placed as close as possible to the oscillator pins, i.e. XTALP_50M and XTALN_50M. C_{int} is the on-chip capacitance between XTALP and XTALN, and it is 5.5pF under the typical condition using default register setting.

$$C_L = \frac{(C_1 + C_{1p}) \times (C_2 + C_{2p})}{(C_1 + C_{1p}) + (C_2 + C_{2p})} + C_{int} \qquad \text{Equation (2.8.2)}$$

Fig. 2.8.2 Crystal Implementation



If an external oscillator is used as the input clock source, the signal must be fed to the XTALP_50M pin only, and XTALN_50M is grounded. Table2.8.2.2 lists the electrical characteristics of the external clock signal. For better performance of the FMCW synthesizer, oscillator frequency of at least 100MHz is highly recommended if an external oscillator is used.

Table 2.8.2 External Clock Specifications

Name	Description	Min	Mid	Max	Unit
Frequency		50	100		MHz
AC Amplitude	AC-coupled	0.5		1.8	Vpp
Phase Noise at 1kHz	Phase Noise referred to 50MHz			-132	dBc/Hz
Phase Noise at 10kHz				-143	
Phase Noise at 100kHz				-152	
Phase Noise at 1MHz				-153	
Phase Noise at 10MHz				-153	
Frequency Tolerance		-50		50	ppm

2.8.3 Serial communication interface (SCI)

Two external pins: RS232_RX and RS232_TX

Table 2.8.3 Electrical Characteristics

	Min	Mid	Max	Unit
f(baud) Supported baud rate at 20 pF		115.200		KHz

2.8.4 Serial peripheral interface specifications

The related parameters about SPI mainly define the SPI timing sequence and communication logic, are shown as Table 2.8.4

Table 2.8.4 SPI Timing Conditions

Input conditions	Min	Mid	Max	Unit
Input rise time	1		3	ns
Input fall time	1		3	ns
Output conditions	**Min**	**Mid**	**Max**	**Unit**
Output load capacitance	2		12	pF

2.8.5 SWD interface specifications

Compatible with the general SWD interface, this interface is used as a debug port.

3. HLK-LD6002C P02 Module Block

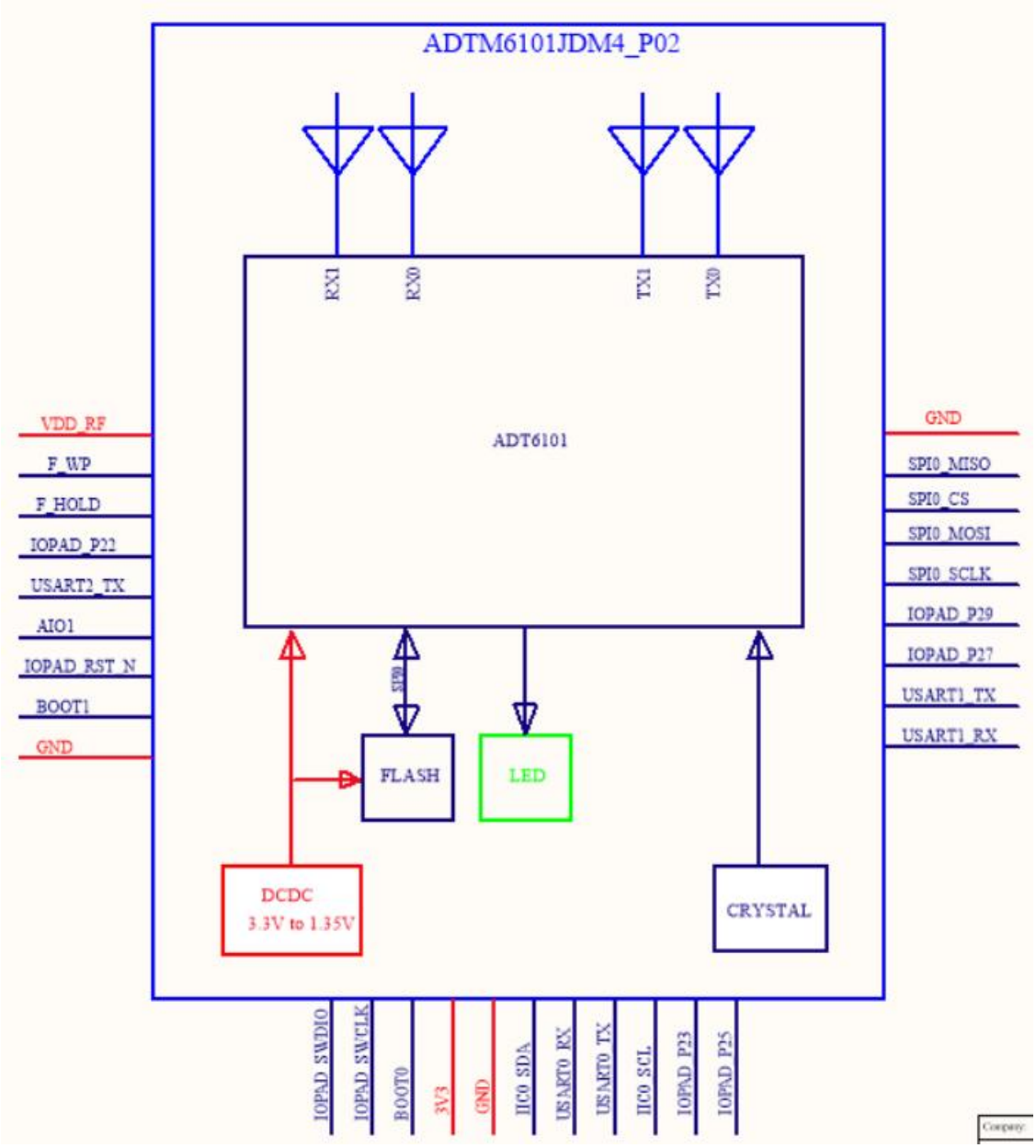


Figure 3-1 HLK-LD6002C module block.

4. HLK-LD6002C Module size

4.1、Top size

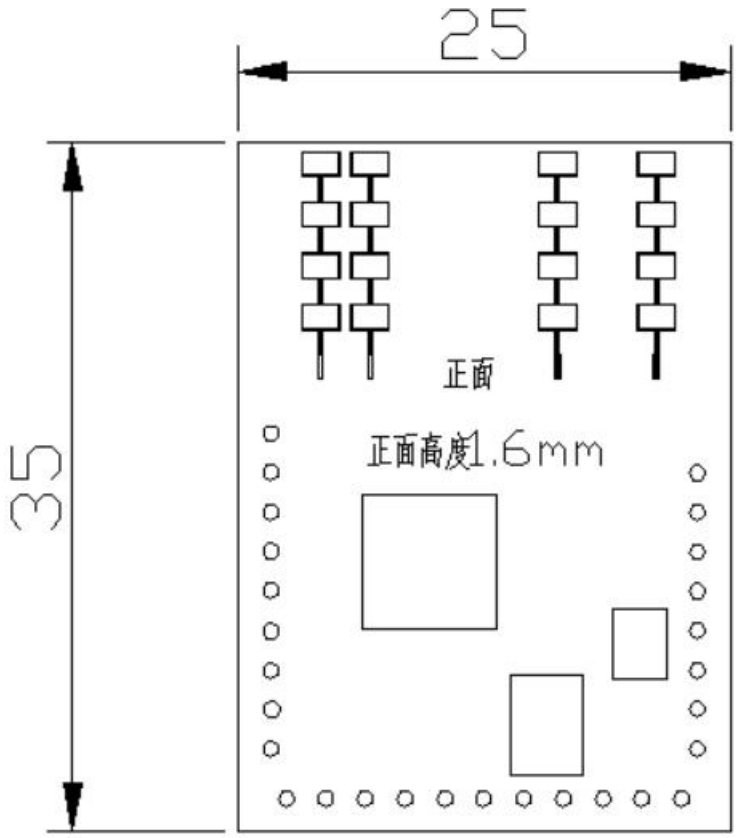


Figure 4-1 HLK-LD6002C module size(unit: mm).

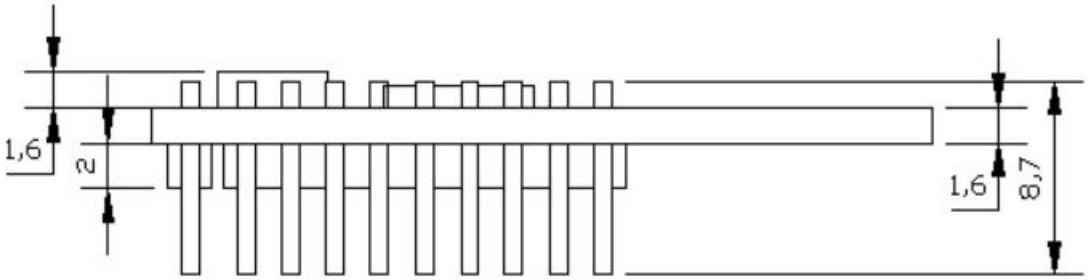


Figure 4-2 HLK-LD6002C module thickness(unit: mm).

4.2、Footprint size

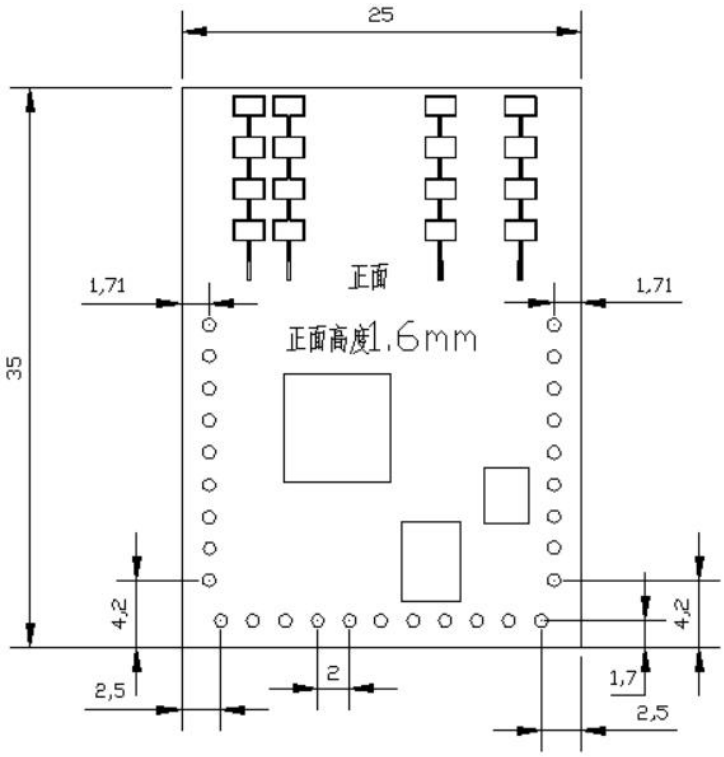


Figure 4-3 HLK-LD6002C module footprint(unit: mm)
(TOP VIEW)

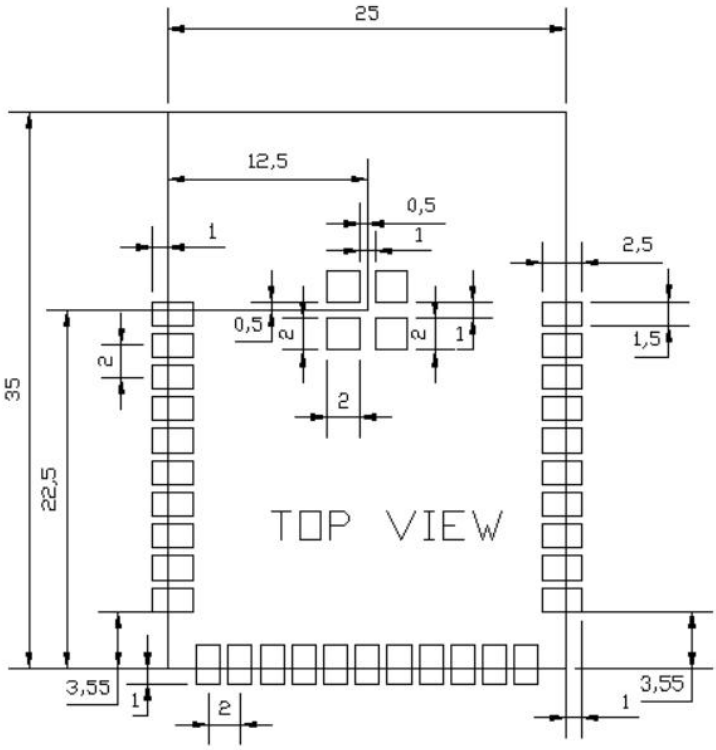


Figure 4-4 HLK-LD6002C module SMT footprint(unit: mm)
(TOP VIEW)

5. HLK-LD6002C Module external interface

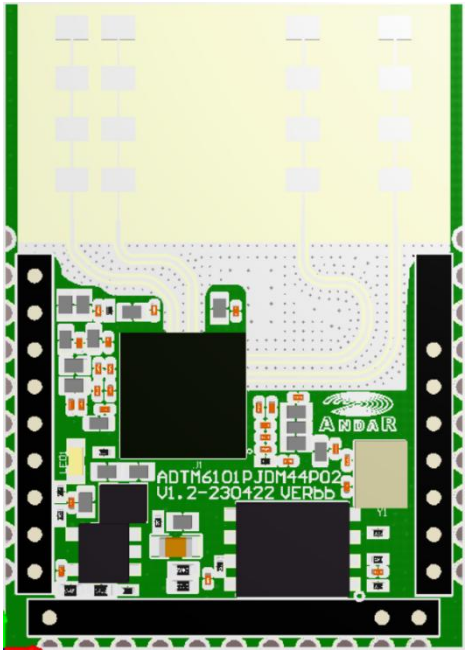


Figure 5.1 package design for 1patch (TOP VIEW)

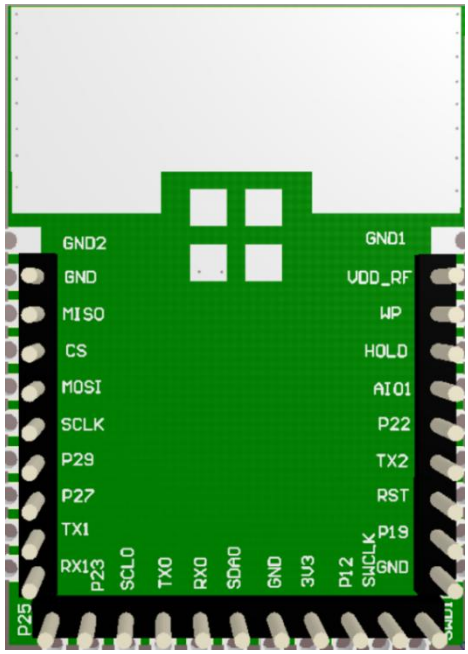


Figure 5.2 package design for 1patch (BOT VIEW)

Table 5.1. 9-Pin interface of left (TOP VIEW)

Pin No.	Pin Name	Description	Notes
GND1	GND	GND	Only support SMT Package
1	VDDRF	External RF Power/1.35V	
2	WP	Write protection active low	Flash function pin
3	HOLD	To pause the device without deselecting the device	Flash function pin
4	AIO1	Temperature index test interface	used as analog input
5	P22	interfaceGPIO_P22/LDO_EXT_EN_H	
6	TX2	GPIO_P20/uart2 txd	control output (such as relay, etc)
7	RST	Reset Signal input	
8	P19	GPIO_P19/boot1	Boot
9	GND0	GND	

Table 5.2. 11-Pin interface of down (TOP VIEW)

Pin No.	Pin Name	Description	Notes
10	SWDIO	SWD Debug Signal	
11	SWCLK	SWD Debug Clock	
12	P12	GPIO_P12/boot0	
13	3.3V	POWER INPUT 3.3V	
14	GND	GND	
15	SDA	GPIO_P08/IIC0_SDA	
16	RX0	GPIO_P01/uart0 _txd	
17	TX0	GPIO_P00/uart0 _txd	

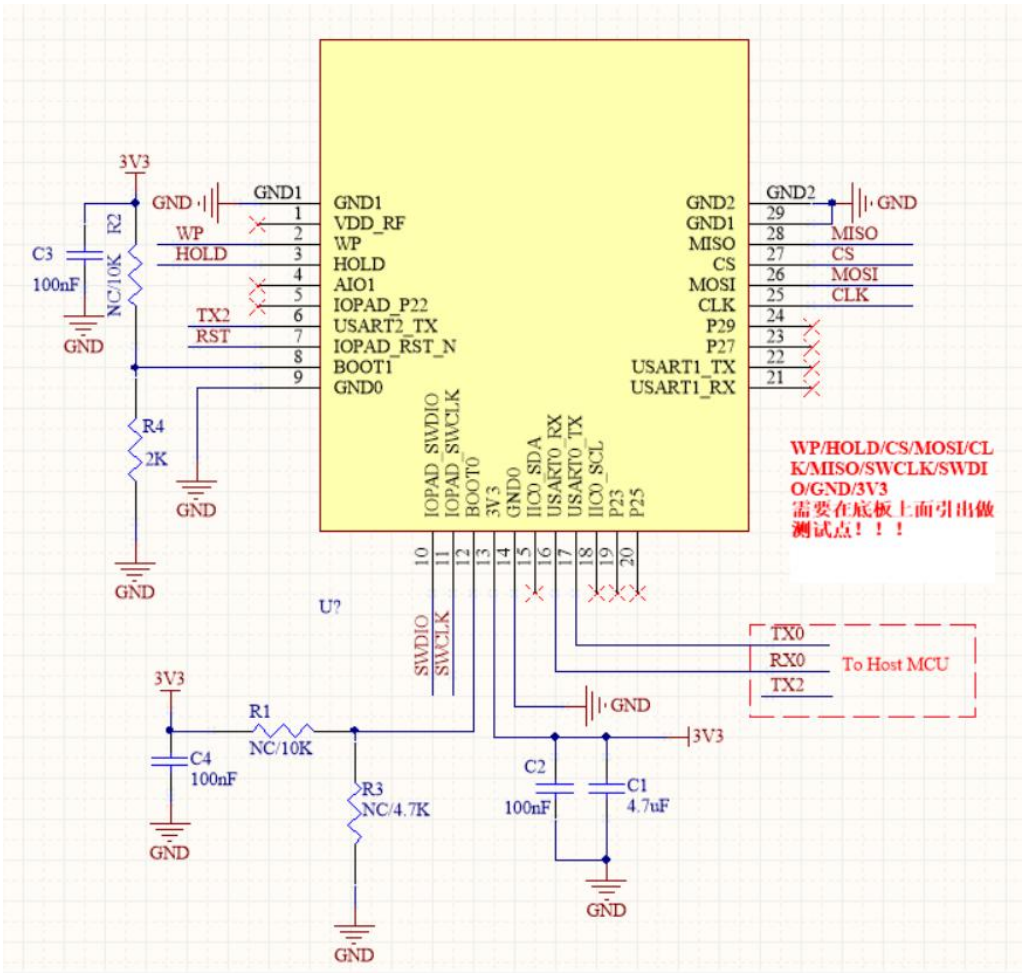
18	SCL	GPIO_P07/IIC0_SCL	
19	P23	IOPAD_P23	
20	P25	IOPAD_P25	

Table 5.3. 9-Pin interface of right (TOP VIEW)

Pin No.	Pin Name	Description	Notes
21	RX1	GPIO_P11/uart1 rxd	
22	TX1	GPIO_P10/uart1 txd	
23	P27	IOPAD_P27	
24	P29	IOPAD_P29	
25	SCLK	IOPAD_P03/SPI0_SCLK	used as an RF ADC signal acquisition output terminal
26	MOSI	IOPAD_P06/SPI0_MOSI	used as an RF ADC signal acquisition output terminal
27	CS	IOPAD_P04/SPI0_CS	used as an RF ADC signal acquisition output terminal
28	MISO	IOPAD_P05/SPI0_MISO	
29	GND1	GND	
GND2	GND2	GND	Only support SMT Package

6、HLK-LD6002C Module Reference Schematic

Figure 6-1 HLK-LD6002C Module Reference Schematic.



Technical support and contact way

Shenzhen Hi-Link Electronic Co., Ltd

Address：17F Building E, Xinghe WORLD, Minzhi Street, Long Hua district, Shenzhen 518131

Phone：0755-23152658/83575155

Email: sales@hlktech.com

Website：https://www.hlktech.net/